IN THE SPECIFICATION

Please replace the paragraph beginning on page 5, line 6 and ending on page 5, line 10 with the following amended paragraph.

In one exemplary embodiment communication module 20 interfaces with microprocessor 24 through a serial connection 22 and ~~to a microprocessor~~interfaces via a microprocessor serial communication port 21 and across an internal/external ~~barrier 25.~~barrier 25 with another device. In an alternate exemplary embodiment communication module 20 interfaces to microprocessor 24 through a parallel connection and to a microprocessor parallel bus.

Please replace the paragraph beginning on page 5, line 20 and ending on page 6, line 3 with the following amended paragraph.

A more detailed sequence of program steps for the initiation of time code transmission is given in Figures 4 and 6. In one exemplary embodiment subroutine 62 is added to the internal clock update routine that incorporates the programming steps below. In an alternate exemplary embodiment the programming steps are added to the clock update code without executing a subroutine. ~~The time and date information is stored in local memory 82 in the main processor such as the Hitachi H8-3644. In an alternate exemplary embodiment the time and date information is stored in local memory outside micro processor 24, such as an EEPROM, part number Microchip 93C66, which then interfaces to microprocessor 24 across internal/external barrier 25. In an alternative embodiment, as illustrated in Figure 5, routine 100 is adapted to read the time information as a block consisting of hours, minutes and seconds, step 102. Microprocessor 24 sends a signal to microprocessor 24 indicating that time information is being transmitted, step 104. Microprocessor 24 transmits the time information to communications module 20, step 106. Microprocessor 24 notifies communications module 20 that data information is being transmitted, step 108. Microprocessor 24 then transmits date information to communications module 20, step 110.~~

Please add the following paragraph after the paragraph beginning on page 5, line 20 and ending on page 6, line 3 and before the paragraph beginning on page 6, line 4 and ending on page 6, line 14.

As shown in Figure 4, subroutine 62 includes reading 64 a time variable, sending 66 time type code to communication module 20, sending 68 time data to communication module 20, reading 70 date variable data, sending 72 date type code to communication module 20, sending 74 date variable data, and sending 76 information from communication module 20 to other appliances. The time and date information is stored in local memory 82 in the main processor such as the Hitachi H8-3644. In an alternate exemplary embodiment the time and date information is stored in local memory outside micro processor 24, such as an EEPROM, part number Microchip 93C66, which then interfaces to microprocessor 24 across internal/external barrier 25. In yet another alternative embodiment, a programmable logic controller device 80 interfaces with communication module 20 via internal/external barrier 25 and microprocessor serial communication port 21. In an alternative embodiment, as illustrated in Figure 5, routine 100 is adapted to read the time information as a block consisting of hours, minutes and seconds, step 102. Microprocessor 24 sends a signal to communication module 20 indicating that time information is being transmitted, step 104. Microprocessor 24 transmits the time information to communication module 20, step 106. Microprocessor 24 notifies communication module 20 that date information is being transmitted, step 108. Microprocessor 24 then transmits date information to communication module 20, step 110.